AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (original) A semiconductor integrated device comprising a ROM decoder of n bits for selecting one gradation voltage out of gradation voltages of the n-th power of 2 gradation in connection with data signals of n bits (n represents an integer of 2 or more ) representing a gradation level, said ROM decoder having n pairs of confronting gate wires each into which the data signal is input with the non-inverted state on one of the pair and with the inverted state on another of the pair,

wherein pairs of the n-th power of 2 each of which comprises an enhancement type transistor and a depletion type transistor kept under ON-state are arranged at predetermined positions one side by one side at the pair of the confronting gate wires, and with respect to each of the pair of the confronting gate wires, the width of the gate wire that contains the upper portion of the depletion type transistor and extends from the depletion type transistor to the enhancement type transistor adjacent to the depletion type transistor is reduced so that recess portions are formed inside the confronting gate wires.

2. (currently amended) The semiconductor integrated circuit device according to claim 1, wherein ~~A semiconductor integrated device comprising a ROM decoder of n bits for selecting one gradation voltage out of gradation voltages of the n-th power of 2 gradation in connection with data signals of n bits (n represents an integer of 2 or more) representing a gradation level, said ROM decoder having n pairs of confronting gate wires each into which the data signal is input with the non-inverted state on one of the pair and with the inverted state on another of the pair,~~

~~wherein pairs of the n-th power of 2 each of which comprises an enhancement type transistor and a depletion type transistor kept under ON-state are arranged at predetermined positions one side by one side at the pair of the confronting gate wires, and with respect to each of the pair of the confronting gate wires,~~ the width of the gate wire that contains the upper portion of the depletion type transistor and extends from the depletion type transistor to the position between the depletion type transistor and the enhancement type transistor adjacent to the depletion type transistor is reduced so that recess portions are formed inside the confronting gate wires.

3. (original) The semiconductor integrated circuit device according to claim 1, wherein with respect to each of the pair of the confronting gate wires, the width of the gate wire between continuously-arranged depletion type transistors is

reduced so that recess portions are formed inside the confronting gate wires.

4. (original) The semiconductor integrated circuit device according to claim 2, wherein with respect to each of the pair of the confronting gate wires, the width of the gate wire between continuously-arranged depletion type transistors is reduced so that recess portions are formed inside the confronting gate wires.

5. (original) The semiconductor integrated circuit device according to claim 1, wherein the reduced width of the gate wire is equal to a half of the gate wire width on the enhancement type transistor.

6. (original) The semiconductor integrated circuit device according to claim 2, wherein the reduced width of the gate wire is equal to a half of the gate wire width on the enhancement type transistor.

7. (original) A liquid display device comprising the semiconductor integrated circuit device according to claim 1.

8. (original) A liquid display device comprising the semiconductor integrated circuit device according to claim 2.

9. (new) A ROM decoder comprising:

at least one enhancement type transistor supplied with a first voltage and having a first gate electrode, said first gate electrode having a first width; and

at least one depletion type transistor coupled to said enhancement type transistor and having a second gate electrode, said second gate electrode having a second width which is smaller than said first width.

10. (new) The ROM decoder as claimed in claim 9, wherein said first gate electrode is supplied with a first data signal and said second gate electrode is supplied with an inverted signal of said first data signal.

11. (new) The ROM decoder as claimed in claim 10, wherein said first gate electrode and said second gate electrode are arranged to overlap a diffusion region, and said first gate electrode of said first width is extended from the overlapped portion into a portion other than said diffusion region while keeping said first width.

12. (new) A ROM decoder comprising:

a plurality of first nodes each supplied with the respective voltages;

a plurality of second nodes coupled to one another;

a plurality of data lines each receiving the respective data signals, each of said data lines being arranged to cross a line between the respective first node and the respective second node, each of said data lines having a pair of gate wires, one of said gate wires receiving a non-inverted digital signal and having a first portion of a first width and a second portion of a second width larger than said first width, the other of said gate

wires receiving an inverted digital signal and having a third portion of a third width and a fourth portion of a fourth width larger than said third width;

a plurality of enhancement type transistors provided to said second and fourth portions; and

a plurality of depletion type transistors provided to said first and third portions.

13. (new) The ROM decoder as claimed in claim 12, wherein

the enhancement type transistor is provided to one of said second and fourth portions on a crossing point of the pair of gate wires and said line,

the depletion type transistor is provided to one of said first and third portions on a crossing point of the pair of gate wires and said line.